

ARRANGEMENT FOR TESTING A NETWORK DEVICE  
BY INTERFACING A LOW SPEED EMULATION SYSTEM  
WITH A HIGH SPEED CPU

ABSTRACT OF THE DISCLOSURE

A system is provided for delaying a ready signal from an emulation system, configured for emulating a network device, to a central processing unit (CPU) for initiating an access cycle of the CPU. The system includes an emulation system and a central processing unit (CPU). The emulation system is configured for operating according to an emulation clock having a maximum speed substantially less than a prescribed operating speed of the CPU. The emulation system includes programmable device configured for receiving a ready signal from the emulation system, delaying the ready signal based on the emulation clock, and sending the delayed ready signal to the CPU based on the emulation clock. The delayed ready signal enables the emulation system to complete the access cycle of the CPU prior to the CPU initiating processing of subsequent instructions.